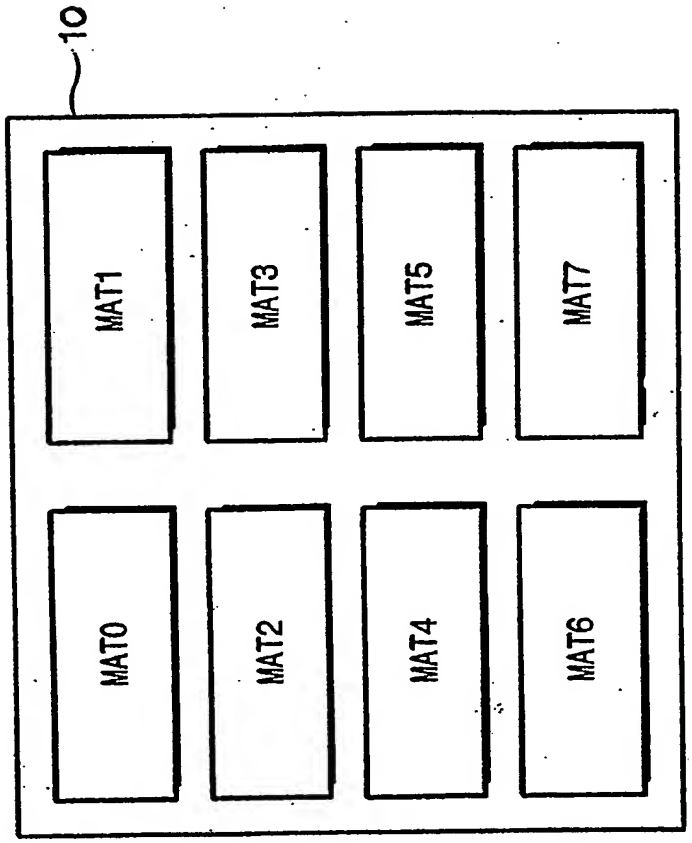


Fig. 1
(PRIOR ART)

Fig. 2
(PRIOR ART)

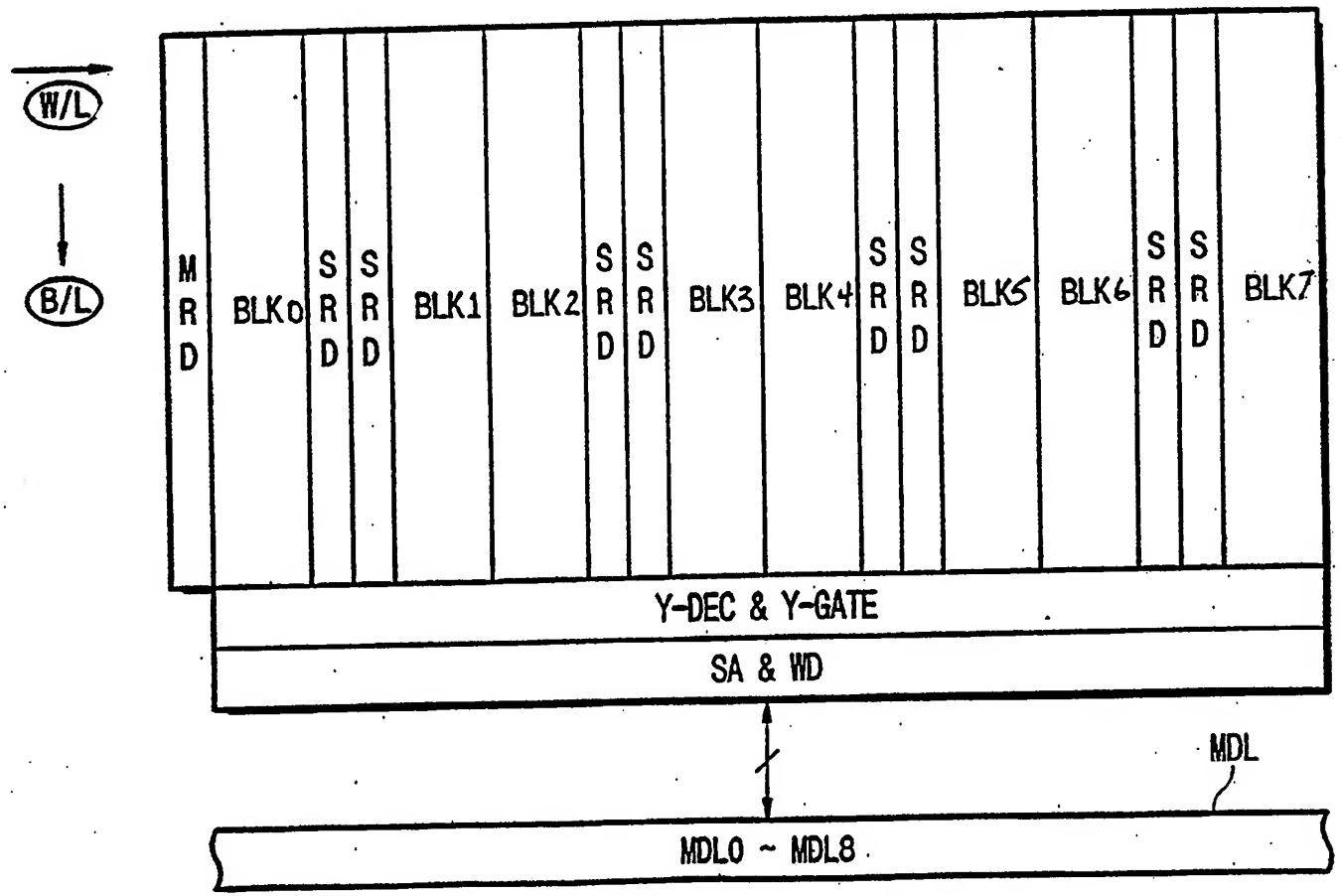


Fig. 3
(PRIOR ART)

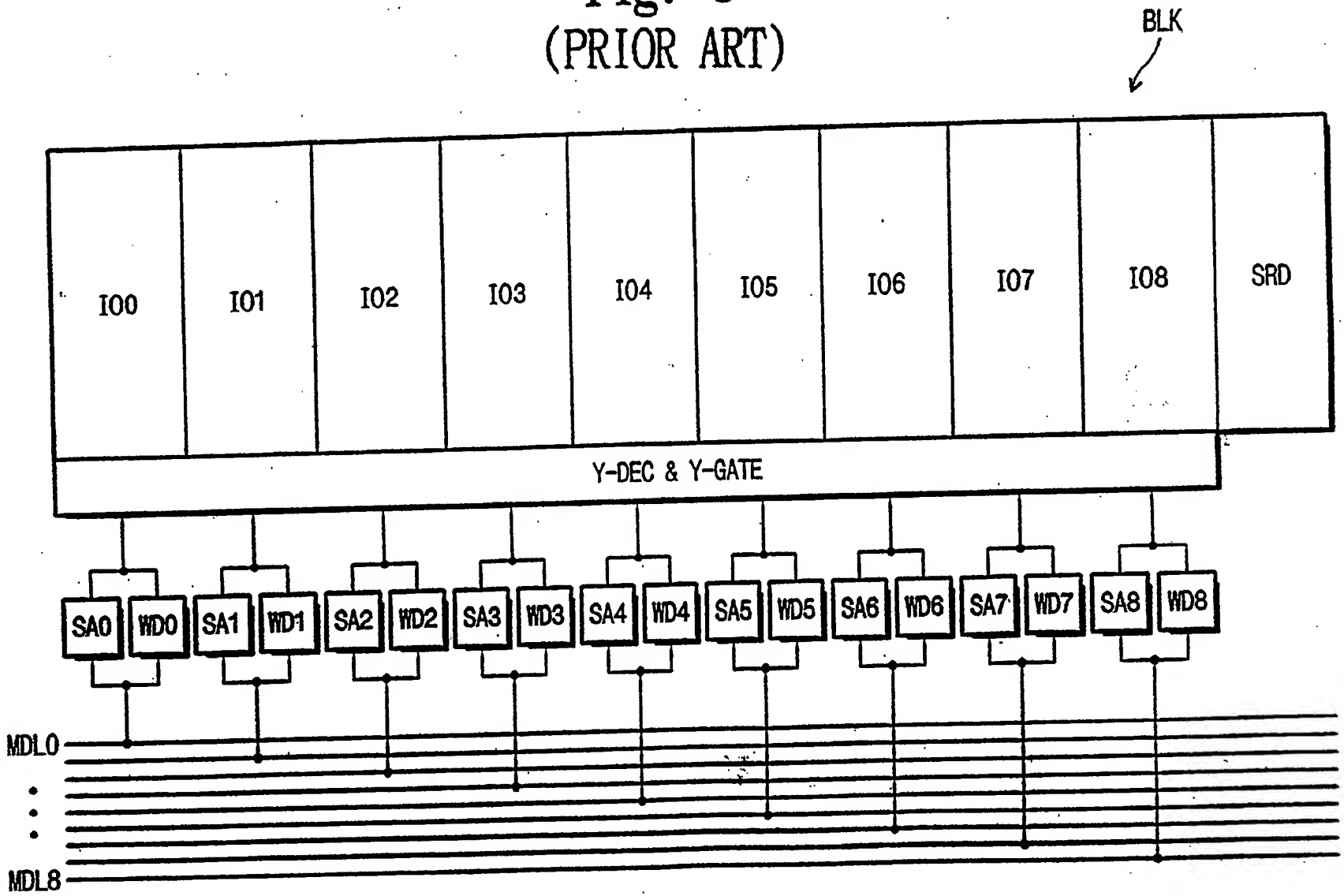


Fig. 4A (PRIOR ART)

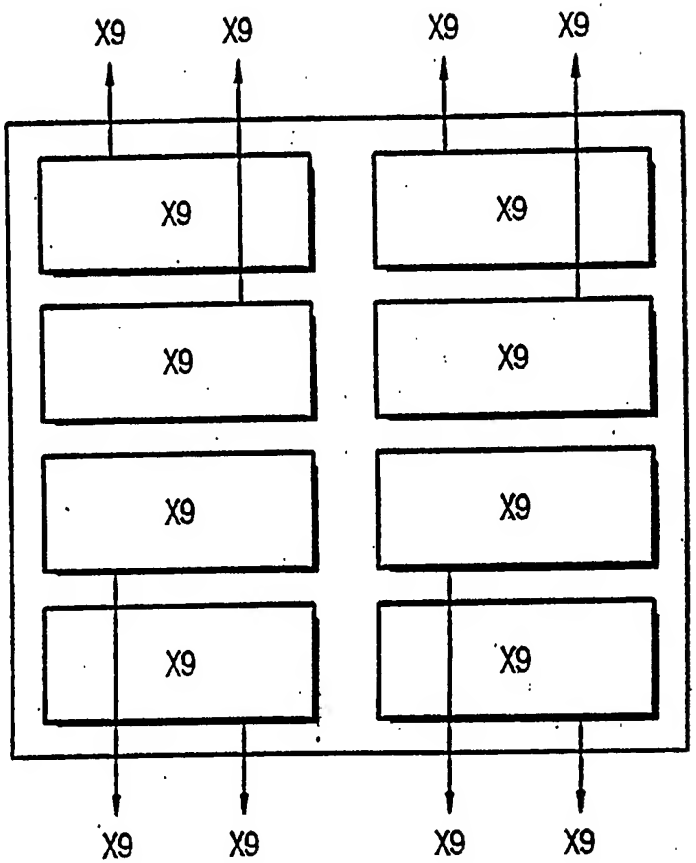


Fig. 4B
(PRIOR ART)

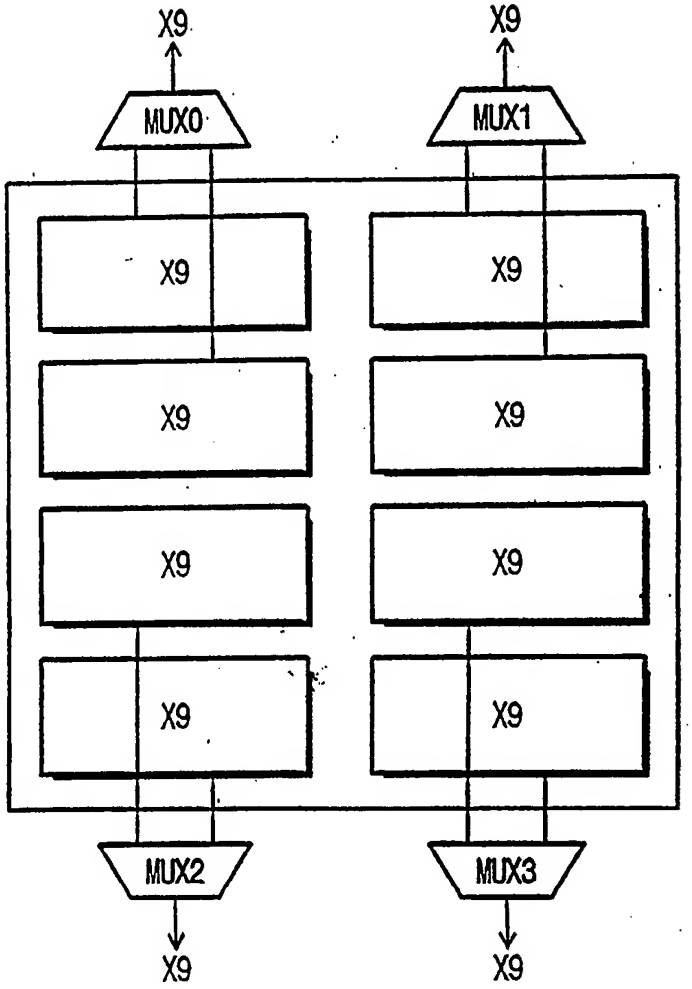


Fig. 4C
(PRIOR ART)

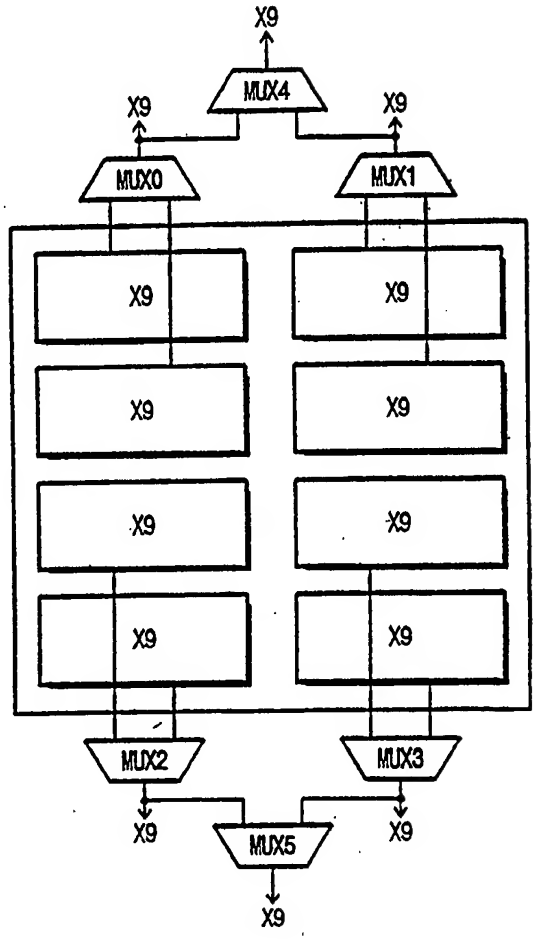


Fig. 5

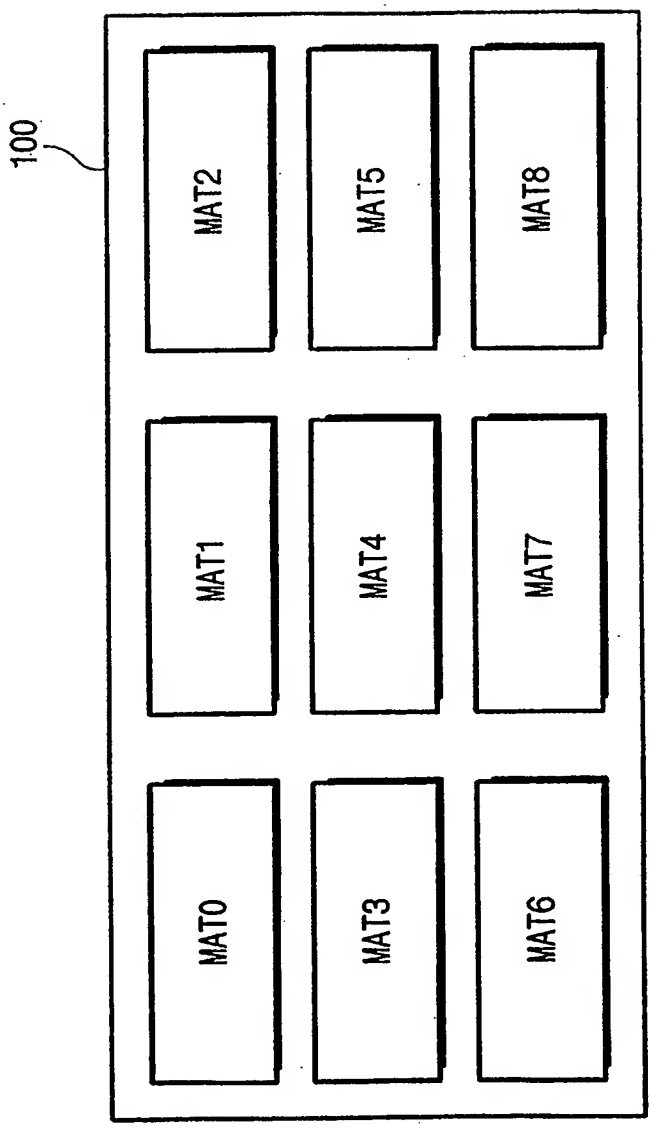


Fig. 6

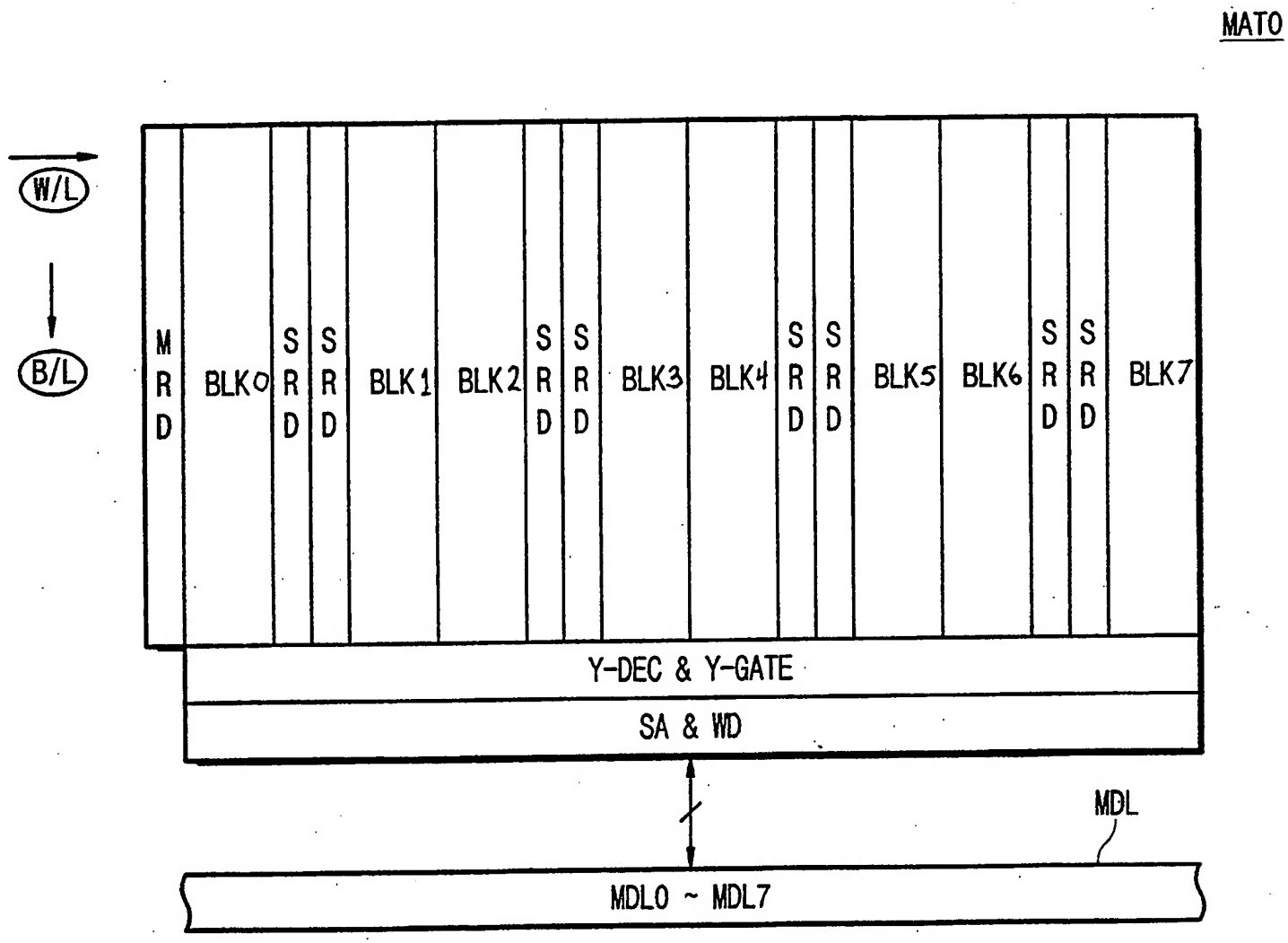

MAT0
W/L
B/L
MRD
BLK0
SRD
SRD
BLK1
BLK2
SRD
SRD
BLK3
BLK4
SRD
SRD
BLK5
BLK6
SRD
SRD
BLK7
Y-DEC & Y-GATE
SA & WD
MDL
MDL0 ~ MDL7

Fig. 7

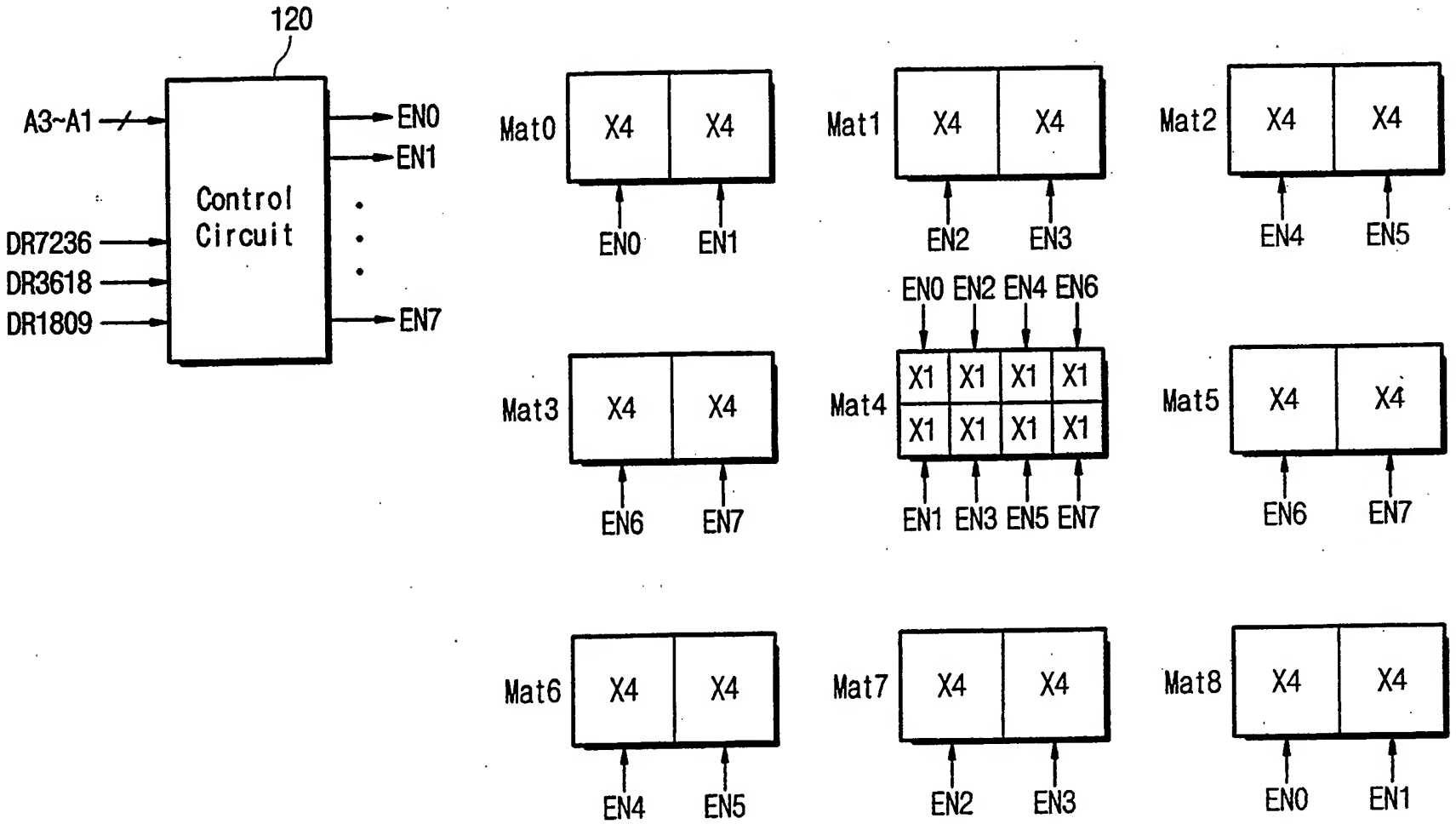

120
A3~A1
DR7236
DR3618
DR1809
Control Circuit
EN0
EN1
EN7
Mat0
X4
X4
EN0
EN1
Mat1
X4
X4
EN2
EN3
Mat2
X4
X4
EN4
EN5
EN0 EN2 EN4 EN6
Mat3
X4
X4
EN6
EN7
Mat4
X1 X1 X1 X1
X1 X1 X1 X1
EN1 EN3 EN5 EN7
Mat5
X4
X4
EN6
EN7
Mat6
X4
X4
EN4
EN5
Mat7
X4
X4
EN2
EN3
Mat8
X4
X4
EN0
EN1

Fig. 8

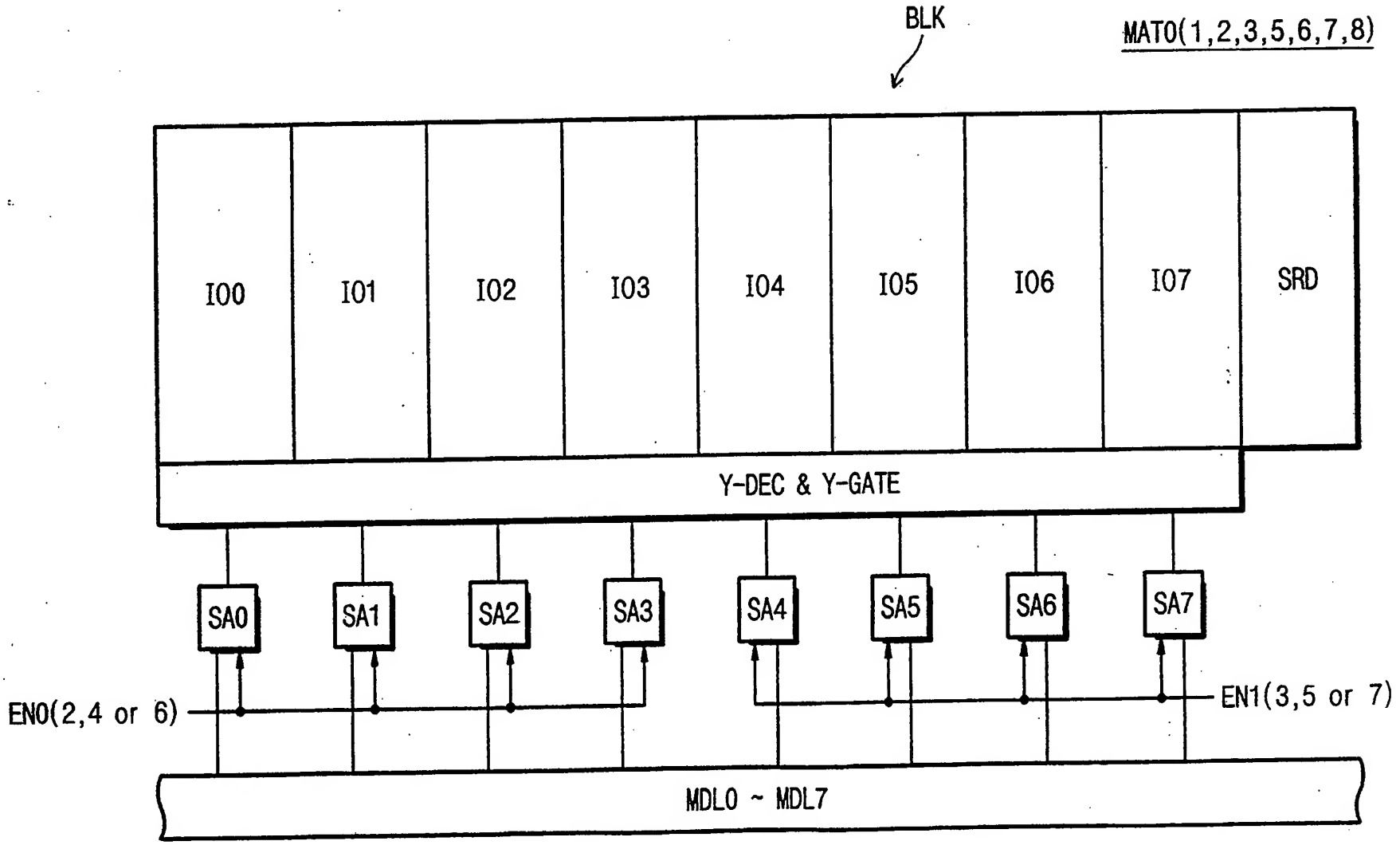

BLK
MAT0(1,2,3,5,6,7,8)
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
SRD
Y-DEC & Y-GATE
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
EN0(2,4 or 6)
EN1(3,5 or 7)
MDL0 ~ MDL7

Fig. 9

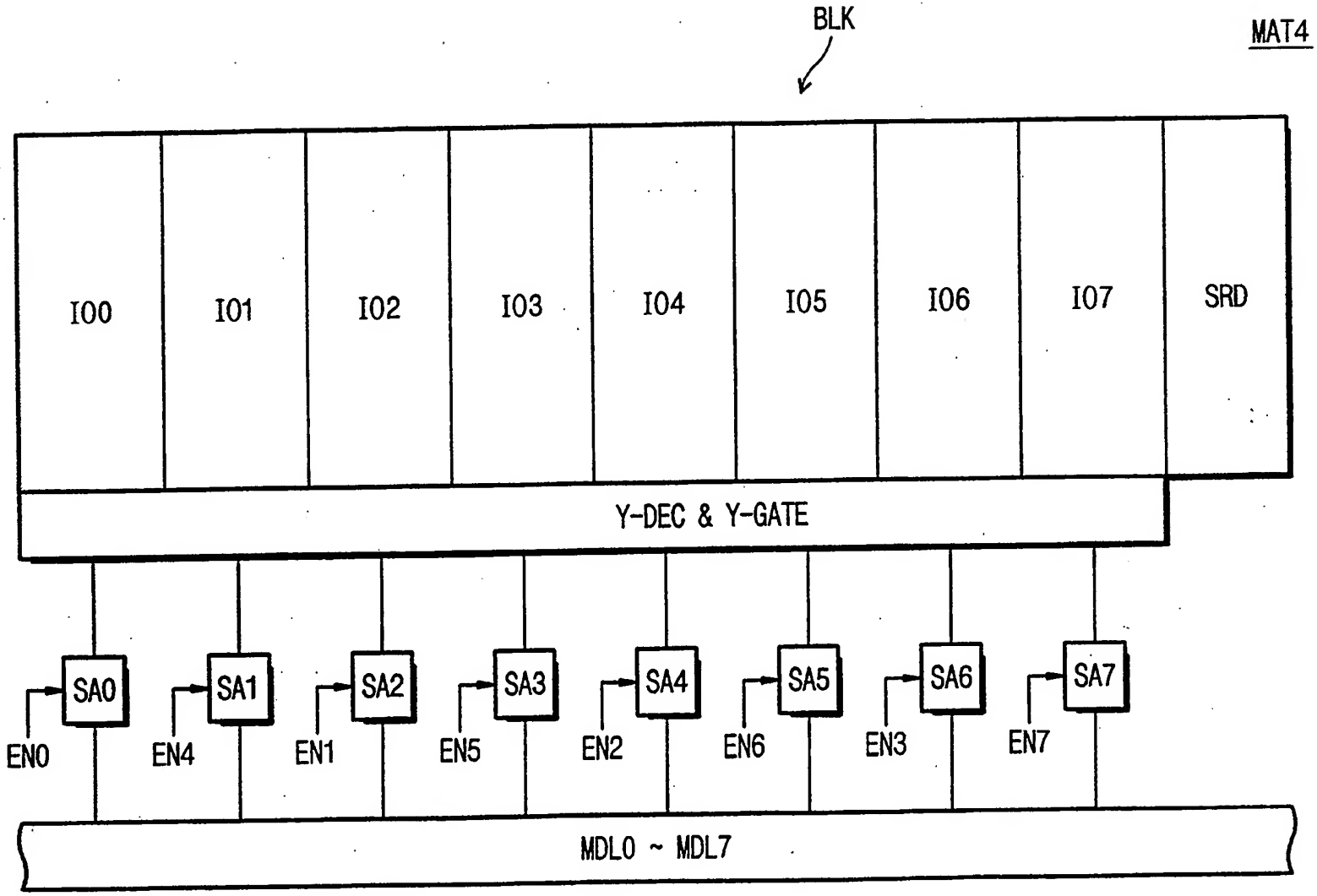

BLK
MAT4
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
SRD
Y-DEC & Y-GATE
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
EN0
EN4
EN1
EN5
EN2
EN6
EN3
EN7
MDL0 ~ MDL7

Fig. 10

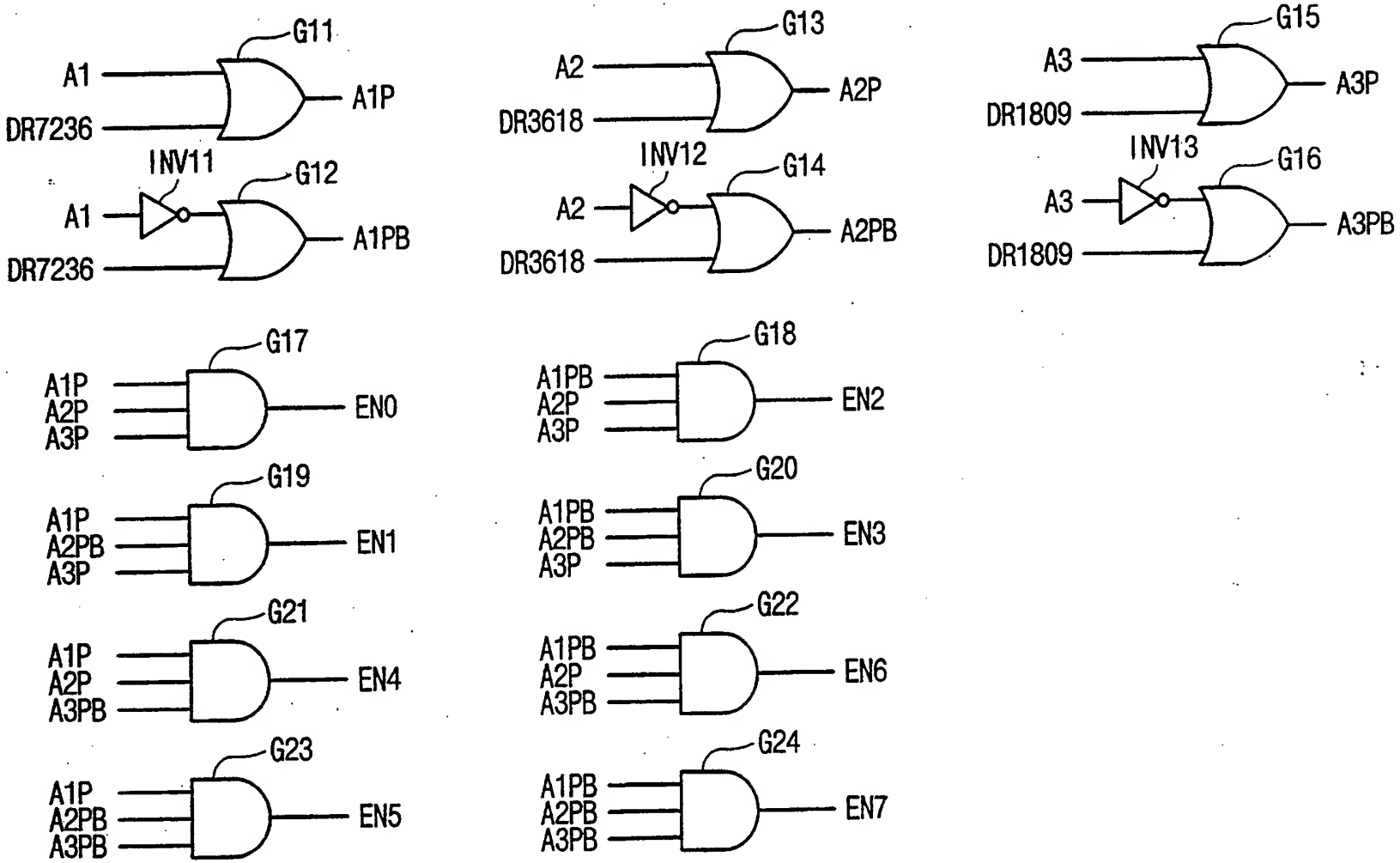
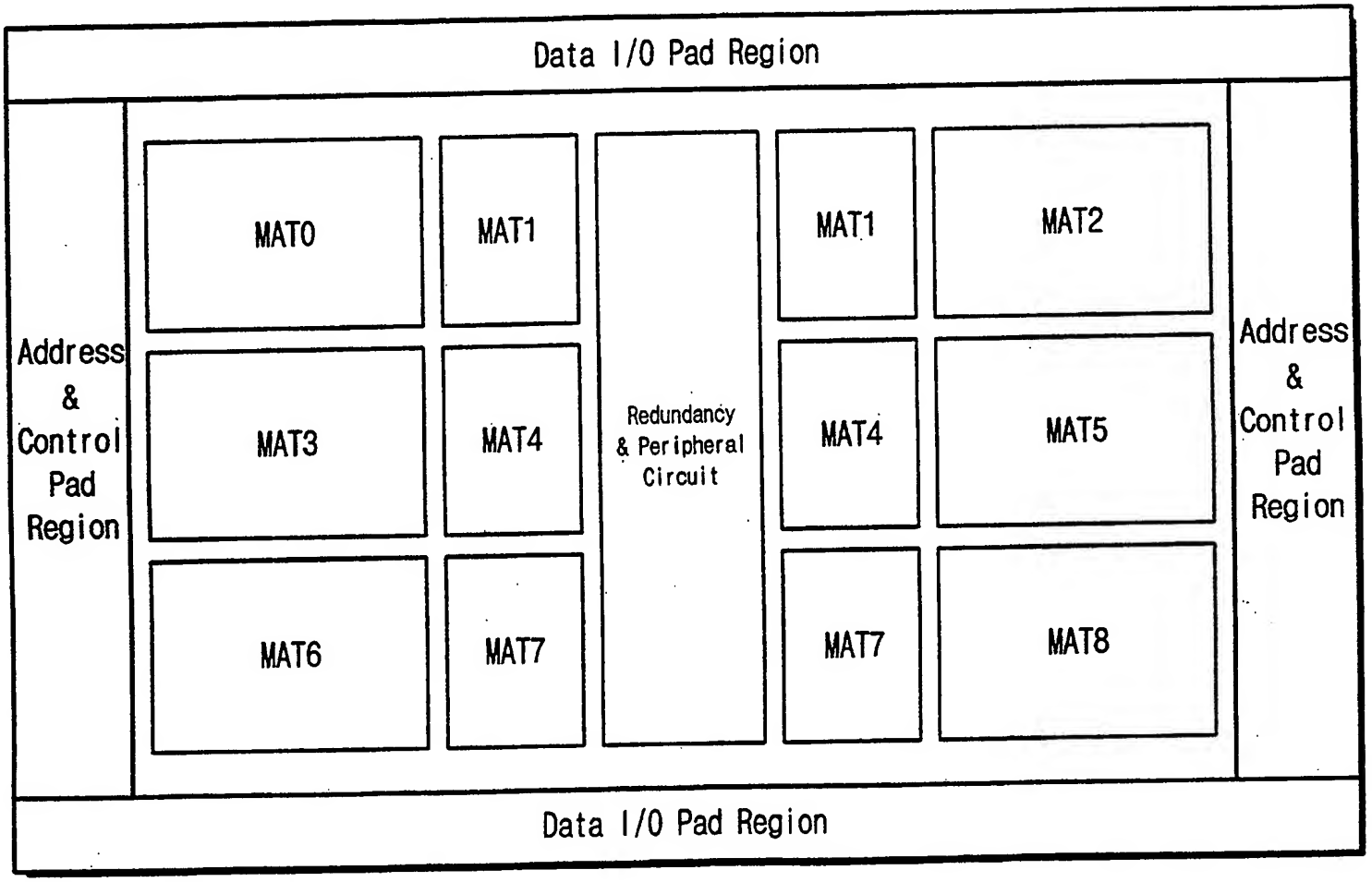

G11
A1
DR7236
A1P
INV11
G12
A1
DR7236
A1PB
G13
A2
DR3618
A2P
INV12
G14
A2
DR3618
A2PB
G15
A3
DR1809
A3P
INV13
G16
A3
DR1809
A3PB
G17
A1P
A2P
A3P
EN0
G18
A1PB
A2P
A3P
EN2
G19
A1P
A2PB
A3P
EN1
G20
A1PB
A2PB
A3P
EN3
G21
A1P
A2P
A3PB
EN4
G22
A1PB
A2P
A3PB
EN6
G23
A1P
A2PB
A3PB
EN5
G24
A1PB
A2PB
A3PB
EN7

Fig. 11


Data I/O Pad Region
Address & Control Pad Region
MAT0
MAT1
MAT3
MAT4
MAT6
MAT7
Redundancy & Peripheral Circuit
MAT1
MAT2
MAT4
MAT5
MAT7
MAT8
Address & Control Pad Region
Data I/O Pad Region